WHAT IS CLAIMED IS:

1. A memory device comprising:

a main controller including a host interface and a device interface;

a first plurality of arrays of magneto-resistive random access memory (MRAM) cells;

a first device controller coupled to the device interface and the first plurality of arrays;

a second plurality of arrays of MRAM cells; and

a second device controller coupled to the device interface and the second plurality of arrays,

wherein the first device controller is configured to communicate with the device interface to pass first data between the first plurality of arrays and the host interface, and wherein the second device controller is configured to communicate with the device interface to pass second data between the second plurality of arrays and the host interface.

2. The memory device of claim 1, wherein the first device controller and the second device controller communicate with the device interface through a serial communication link.

3. The memory device of claim 2, wherein the first device controller converts a first serial signal into a first parallel signal for writing to the first plurality of arrays of MRAM cells, and wherein the second device controller converts a second serial signal into a second parallel signal for writing to the second plurality of arrays of MRAM cells.

4. The memory device of claim 1, wherein the main controller includes a spare table for storing original addresses of defective memory sections within the first plurality of arrays and the second plurality of arrays.

5. The memory device of claim 4, wherein the spare table stores spare addresses to use in place of the original addresses of defective memory sections within the first plurality of arrays and the second plurality of arrays.

6. The memory device of claim 1, wherein the host interface is configured to pass the first data between the main controller and an external device.

7. The memory device of claim 6, wherein the host interface is configured to pass the first data between the main controller and the external device through one of a serial and parallel communication bus.

8. The memory device of claim 7, wherein the one of the serial and parallel communication bus comprises one of a Small Computer System Interface (SCSI), Integrated Drive Electronics (IDE), Serial AT Attachment (SATA), Industry Standard Architecture (ISA), Personal Internet Client Architecture (PCA), Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), and InfiniBand bus.

9. The memory device of claim 1, wherein the main controller includes a data buffer to temporarily store the first data as the first data is passed between the device interface and the host interface.

10. The memory device of claim 9, wherein the main controller includes a data mover configured to control the passing of the first data between the host interface and the data buffer and between the data buffer and the device interface.

11. The memory device of claim 1, wherein the main controller includes a microprocessor configured to execute instructions for controlling the host interface and the device interface.

12. The memory device of claim 1, wherein the first plurality of arrays are coupled in parallel and the second plurality of arrays are coupled in parallel.

13. The magnetic memory storage device of claim 1, wherein the device interface comprises an error detection and correction circuit for encoding and decoding the data.

14. The memory device of claim 1, wherein the main controller is fabricated entirely on a semiconductor chip.

15. The memory device of claim 1, wherein the first plurality of arrays, the second plurality of arrays, the first device controller, and the second device controller are fabricated entirely on a semiconductor chip.

16. The memory device of claim 1, wherein the main controller, the first plurality of arrays, the second plurality of arrays, the first device controller, and the second device controller are fabricated entirely on a semiconductor chip.

17. A system comprising:

a host;

a storage device coupled to the host, the storage device comprising:

a main controller having a device interface;

a magneto-resistive random access memory (MRAM) comprising a first device controller coupled to a first plurality of arrays of memory cells and a second device controller coupled to a second plurality of arrays of memory cells;

a host interface; and

a housing at least partially enclosing the main controller, the magneto-resistive random access memory, and the host interface,

wherein the main controller is configured to pass data between the first device controller and the device interface, between the second

device controller and the device interface, and between the device interface and the host interface.

18. The solid state memory device of claim 17, wherein the host interface is configured for removable coupling to the host.

19. The solid state memory device of claim 17, wherein a storage capacity of the MRAM is scalable.

20. The solid state memory device of claim 17, wherein a data transfer rate of the MRAM is scalable.

21. The solid state memory device of claim 17, wherein the housing is one of a 5.25 inch, 3.5 inch, 2.5 inch, 1.8 inch, 1.3 inch, and 1 inch form factor.

22. A storage device comprising:

first means for receiving first addresses and first data;

second means for converting the first addresses and the first data to a first serial data stream;

third means for transmitting the first serial data stream to a magneto-resistive random access memory (MRAM);

fourth means for converting the first serial data stream to second addresses in a parallel format and second data in the parallel format; and

fifth means for writing the second data to the second addresses in the MRAM.

23. The storage device of claim 22, further comprising:

sixth means for reading third data in the parallel format using third addresses in the parallel format in the MRAM;

seventh means for converting the third parallel data to a second serial data stream; and

eighth means for transmitting the second serial data stream to the first means.

24. A method for writing data to a magneto-resistive random access memory (MRAM) device comprising:

receiving data and logical block addresses from a host;

translating the logical block addresses to physical block addresses;

transmitting the data and physical block addresses in a serial data stream to an MRAM;

converting the serial data stream to parallel physical block addresses and parallel data; and

storing the data to the physical block addresses in the MRAM.

25. The method of claim 24, further comprising:

comparing the physical block addresses to original addresses of defective memory sections stored in a spare table; and

replacing the physical block addresses with replacement addresses stored in the table based upon the comparison.

26. The method of claim 24, further comprising:

encoding the data using an error detection and correction circuit.

27. A method for reading data from a magneto-resistive random access memory (MRAM) device comprising:

receiving logical block addresses from a host;

translating the logical block addresses to physical block addresses;

transmitting the physical block addresses in a serial data stream to an MRAM;

converting the serial data stream to parallel physical block addresses;

reading data from the physical block addresses in the MRAM;

converting the read data to a serial data stream;

transmitting the serial data stream to a device interface; and

passing the data to the host.

28. The method of claim 27, further comprising:

comparing the physical block addresses to original addresses of defective memory sections stored in a spare table; and

replacing the physical block addresses with replacement addresses stored in the spare table based upon the comparison.

29. The method of claim 27, further comprising:

decoding the data using an error detection and correction circuit.